Power Supply Design Guidelines

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Revision	Description	Date
0.1	Initial DRAFT	31/07/05
0.2	Correction equations 9 and 11	15/09/05
0.3	Changed document template	13/04/11

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1. Overview

1.1. General

The purpose of this document is to introduce general design guidelines and knowledge on power supply design methodologies and considerations. Most of the topologies shown in this document relate to step-down power supplies, though step-up is shown also for common knowledge.

The reader of this document will achieve the following:

- Basic knowledge on AC/DC power supply units
- Basic/Intermediate level of knowledge on DC/DC power supply units
- Power supply topology design abilities for specific requirements of specific systems
- Understanding the trade-offs of the design topology
- Selecting the required components and calculate their values
- Controlling the output noise and ripple
- A complete power supply design

These guidelines are based mostly on the following:

- Datasheets
- Application Notes
- Articles on Power Supplies
- Power Supply Consultant instructions and guidelines
- Previous Power Supply Designs

2. Step Down Topologies

A power supply is a buffer circuit that is placed between an incompatible power source and a load in order to make them compatible.

Contemporary designs are usually generated of a single voltage power source, from which the PCB is fed. The various voltages required by the components on the PCB are generated in various methods, which are summarized as follows:

2.1. Linear Regulators, (LDO – Low Drop Regulator)

This is a linear solution. Figure 1 shows the Regulator Operation.

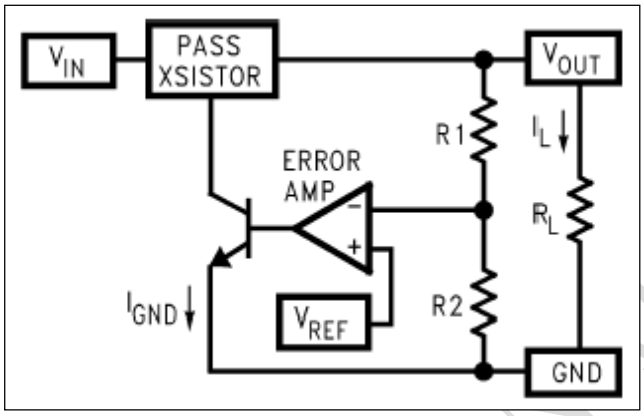

Figure 1: Voltage Regulator

The output voltage is sampled, (measured), through a resistor divider which is fed into the inverting input of an error amplifier. The non-inverting input is tied to a reference voltage. The error amplifier will always try to force the voltages at its input to be equal. To do this, it sources current as required to provide sufficient load current to maintain the output voltage at the regulated value, which is given by Vout = Vref (1+R1/R2).

The resistors R1 and R2 maybe external in adjustable LDO versions, or internal with fixed output LDOs.

Typical Vref is about 1.25V depending on the component and technology.

2.1.1. Advantages

- Low parts count and easy to design
- Cheap
- Excellent regulation characteristics
- Low output noise
- No generated EMI
- Excellent transient response

2.1.2. Disadvantages

- Single Output
- No Step-Up designs
- Poor efficiency, especially in high ΔV x I = (Vout-Vin) x I
- Sometimes requires heat sinks as part of the PCB or external heat sinks.

2.2. Switched Power Supplies - Intro

When higher efficiencies are required, one must apply a switched power supply topology.

2.2.1. Forward

- The concept of switching is based on transferring energy from the main power supply source to the load during a time slot, (pulse width). In order to maintain a DC voltage for the load, this energy is averaged, and the voltage ripple is minimized.
- The time slot, in which the energy is transferred, is increased on heavy loads and decreased on lighter loads.
- The switching frequency range is 50kHz to about 2MHz.
- The switching circuitry is employed of a switching controller, a low series resistant Transistor/FET, low ESR inductor/transformer, low ESR capacitor and an output voltage correction loop. (Current limit and protection circuits are also applied).
- The efficiency ranges between 70% to 95%, depending on topology, Vin, Vout, and the loss on the components.

2.2.2. Common Topologies

The topologies are divided into three types:

- Step down – Relates to a power supply where Vout<Vin
  - Flyback – discussed shortly on Chapter 3.
  - Buck – discussed on Chapter 4
  - Synchronous Buck – discussed on Chapter 5
- Step Up – Relates to a power supply where Vout>Vin, (not in scope of this document)
  - Boost
- Step Up/Down – Relates to a power supply where Vout is greater or smaller than Vin, (not in scope of this document)
  - Buck-Boost
  - SEPIC

2.2.3. Switching Frequency and Size

The physical size of power-switching and energy storage elements in switching DC/DC converters is directly affected by the operating frequency. The power coupled by a magnetic element is:

$$P(L) = \frac{1}{2} \cdot L \cdot I^2 \cdot f$$

Equation 1: Power coupled by a magnetic element

As operating frequency rises, the inductance required to maintain a constant power decreases proportionally. Since inductance is related to the area of magnetic material and number of turns of wire, the physical size of an inductor can be decreased.

In other words, the higher the frequency the smaller the inductor's physical dimensions.

3. Switching in AC/DC power supplies

3.1. AC/DC Power Supplies

This chapter shows the concept of switching related to an AC/DC power supply.

3.1.1. Legacy AC/DC Power Supplies

Legacy, non-switched, power supplies were based on a 220V/110V input voltage, an input stage transformer with a 1:X winding ratio, a bridge rectifier, and an output Low Pass Filter, as shown in Figure 2. In order to comply with output voltage regulation smaller than 15%, an additional linear regulator is required.

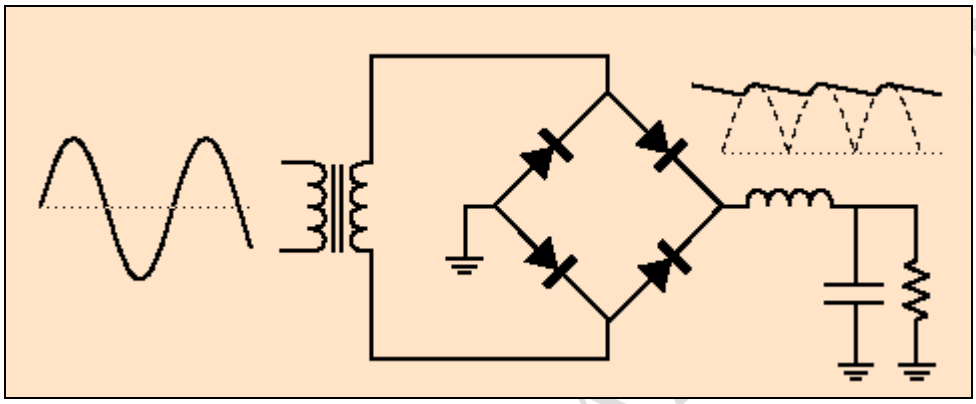

Figure 2: Legacy AC/DC Power Supplies

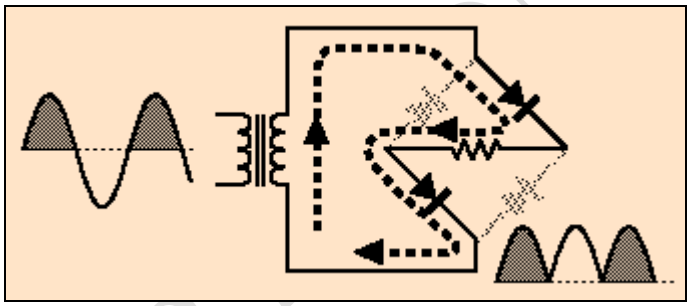

Figure 3: Current flow in the Bridge Rectifier for Positive Swing

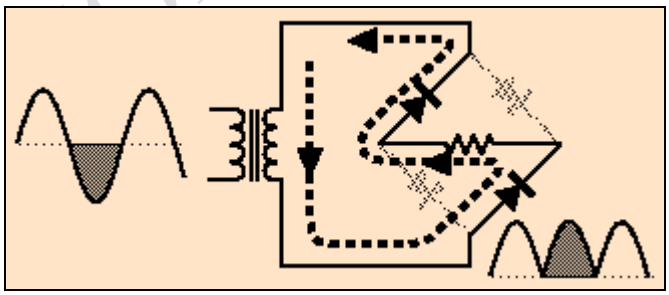

Figure 4: Current flow in the Bridge Rectifier for Negative Swing

For multiple output voltages, multiple output transformers are used, and output stage Low Pass Filters are added for each stage.

3.1.1.1. Advantages

- Simple
- 50/60Hz transformers are robust and compliant with safety regulations
- The output ripple is 50/60Hz, (and the related harmonics)

3.1.1.2. Disadvantages

- Large PCB Real Estate - Due to the use of 50/60Hz transformers
- Heavy
- Additional linear regulation is required due to the poor stability of the input 220/110V voltage, (±15%). For ±5% stability requirements on contemporary circuits, this regulator is a must.

Leading to switched Power Supplies.

3.1.2. Switched AC/DC Power Supplies

In order to minimize the PCB Real Estate the following concepts are applied:

- The transformer size increases as the operation frequency decreases and vice versa, (Clause 2.2.3).
- So, by increasing the switching frequency at the output, the transformer at the output would be smaller.
- In order to increase the output frequency, the input voltage should be rectified, and should be DC as possible

Figure 5 shows the application of this concept:

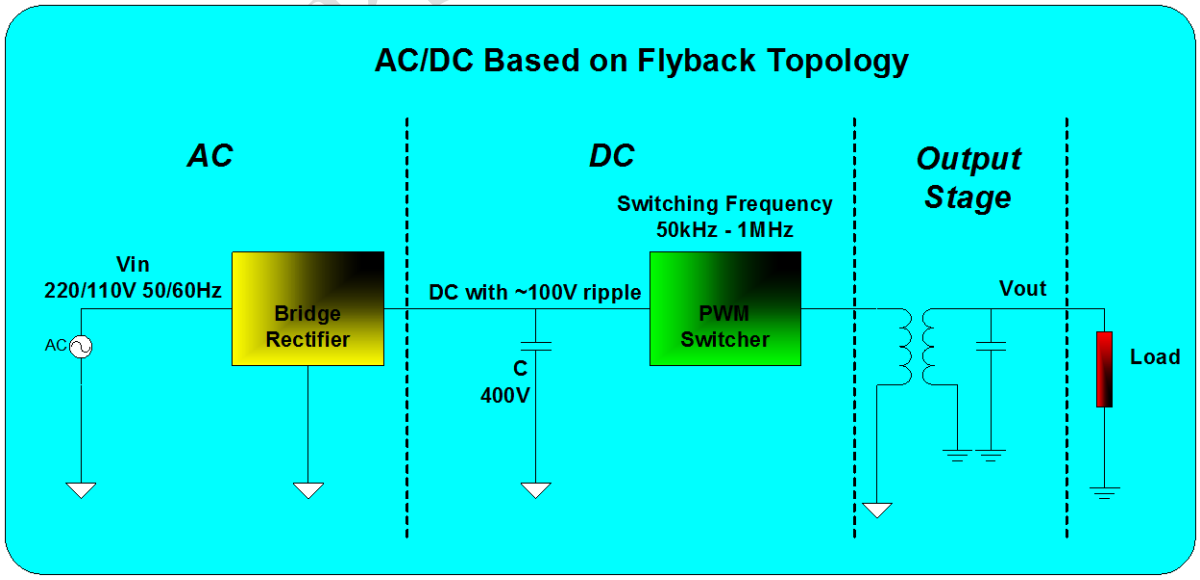

Figure 5: Switched AC/DC Power Supply – Flyback Topology

- The voltage on the High Voltage Capacitor is shown in Figure 5. One can see that although it's not a flat DC, it's flat enough to operate with a PWM switcher

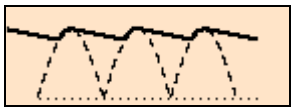

Figure 6: Switched AC/DC Power Supply – Voltage on the Capacitor

- The Capacitor C is physically small since it allows high ripple voltage. The operation voltage is about 400V, (220V x √2 = ~312V).
- Multiple outputs may be as well achieved with multiple output transformers.
- Note that the Flyback topology is used not only in AC/DC power supplies but also in DC/DC supplies. The Flyback section of the AC/DC described above converts a high DC voltage to a lower DC voltage

3.1.2.1. Advantages

- Small output magnetic element, (due to high frequency switching)
- Small Input capacitor C due to relatively high voltage ripple, about 100V
- Total PCB Real Estate and weight
- Isolation due to the Flyback topology, (is a must in AC/DC power supplies).

3.1.2.2. Disadvantages

- More complex design
- Output ripple frequency depends on the switching frequency
- EMI generation

4. PWM, (Pulse Width Modulation), Buck Topology

4.1. Forward

A Buck converter, also known as a Step-Down converter, is one of the common topologies for DC/DC conversion.

It's based on a PWM controller, which controls the duration of the time in which a switch, a Transistor/FET, will be "ON" and "OFF". Hence, the amount of energy transferred from the main power supply towards an energy storage component, Inductor, is controlled.

The control is operated by an output feedback circuitry that samples the variations in the output voltage. These variations are both Vin and load dependent.

On high loads and/or lower Vin, the output voltage will drop, hence the "ON" time duration will be increased. On light loads and/or higher Vin, the "OFF" time duration will be increased.

4.2. Buck Converter - Basic Schematics

Figure 7 shows the basic schematics of a Buck Converter, and the "ON"/"OFF" states of the switch Q1.

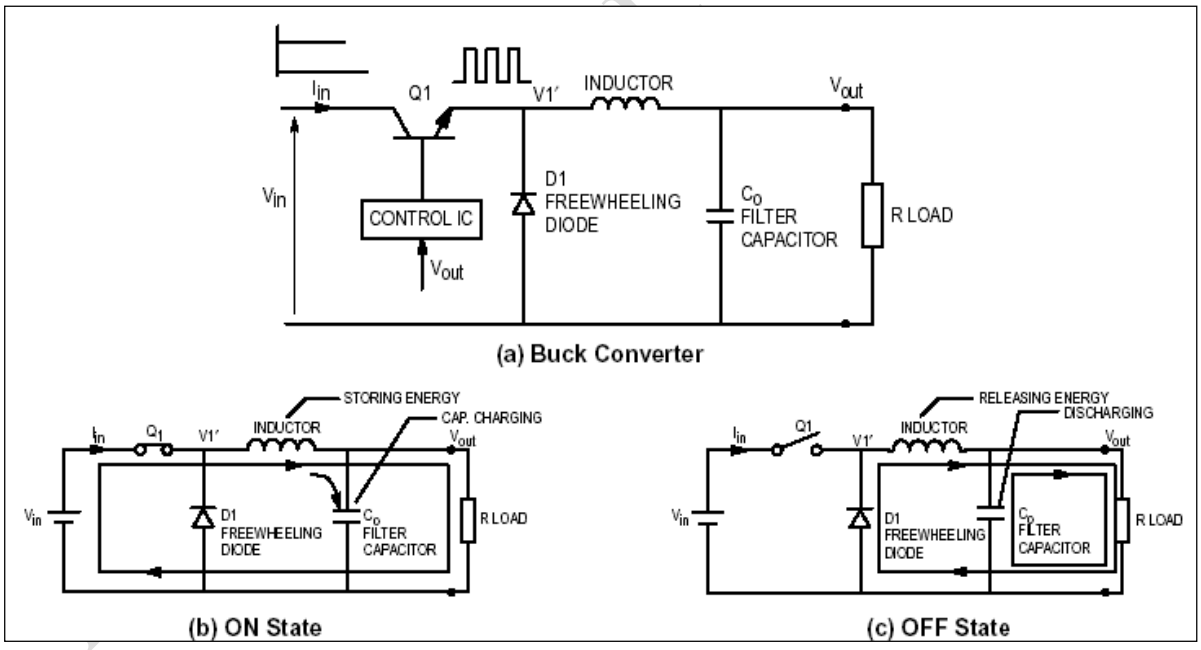

Figure 7: The Buck Converter

When the switch Q1 is turned on, the input voltage is applied to the inductor, and power is then delivered to the output, also energy is stored in the inductor and capacitor Co is charged.

When the switch is turned off, the voltage across the inductor reverses and the free-wheeling diode D1 becomes forward biased. This allows the energy stored in the inductor to be delivered to the output while the continuous current is then smoothed by the output capacitor. Typical waveforms are shown below in Figure 8.

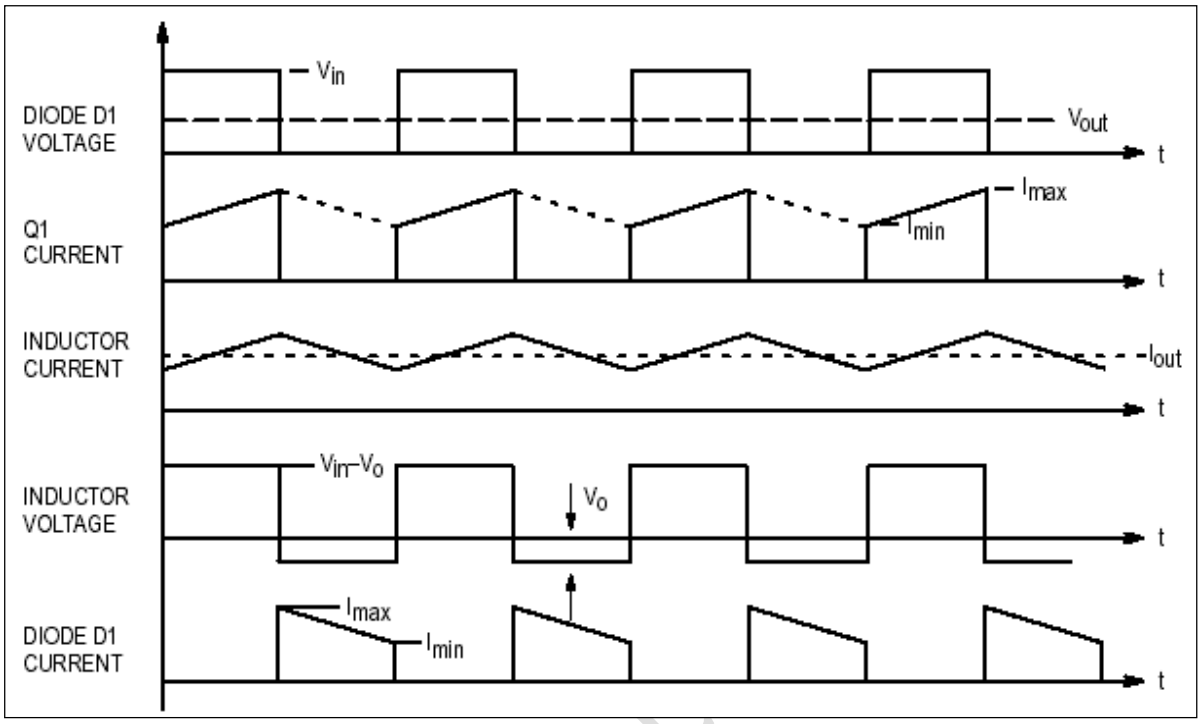

Figure 8: Current and voltage waveforms of the Buck Converter

4.3. Buck Converter Equations

4.3.1. Developing Buck Converter Equations

The voltage across the inductor equals to:

$$V_L = V_{in} - V_{out} = L \cdot \frac{di}{dt}$$

Equation: 2

Solving for $L \cdot di$, we'll get the following:

$$L \cdot di = \int_{ON} (V_{in} - V_{out})dt + \int_{OFF} (V_{in} - V_{out})dt$$

Equation: 3

For steady state operation the current at the start and end of a period T will not change, hence, $di = 0$. To get a simple relation between voltages we assume no voltage drop across the transistor Q1 or the diode D1 while "ON", and a perfect switch change. Thus, during the "ON" time Vin = Vout and in the "OFF" Vin = 0, hence the results will be as follows:

$$L \cdot di = 0 = \int_{0}^{t_{"ON"}} (Vin - Vout)dt + \int_{t_{"ON"}}^{t_{"ON"}+t_{"OFF"}} (-Vout)dt$$

Equation: 4

Resulting:

$$(V_{in} - V_{out})t_{"ON"} - V_{out}t_{"OFF"} = 0$$

Equation: 5

Hence, solving for the duty cycle D will result in:

$$\frac{V_{out}}{V_{in}} = \frac{t_{"ON"}}{T} = D$$

Equation: 6

4.3.2. Conclusions on Buck Converter Equations

- Equation 6 shows a very important relationship between the desired output voltage and the input power supply voltage. One can see that the output voltage depends on the input voltage and the duration of time in which the energy is delivered from the input to the output during the "ON" time.
- Note that the "ON" time will not be the same for different switching frequencies f, or switching periods T.
- This also shows that not every switching frequency can be used for every application. This issue will be further discussed on the chapter 6, the Synchronous Buck Converter Design.

4.3.3. Advantages

- Up to 85% efficiency, depending on Vin, Vout and switching frequency

4.3.4. Disadvantages

- PCB Real Estate
- Complex design
- Output ripple and noise greater than LDO outputs
- Generated EMI

5. Synchronous Buck Topology

5.1. The motivation towards the Synchronous Buck Topology

- In order to increase the efficiency achieved in the Buck Topology, the transistor Q1 is replace by a FET called as "Main switching MOSFET" and the free-wheeling diode D1 is replaced by a "Synchronous Rectifier" FET. The PWM Controller, in this new arrangement, must control the switching of both FETs.
- Note that the FETs must be in "ON" state one at a time only. They must not be "ON" simultaneously.
- This topology is also known as Synchronous Rectifier.
- In order to further minimize the power loss and increase the efficiency, during the dead time when switching between one FET to the other, a Schottky free-wheeling diode is added in parallel with the synchronous rectifier FET.
- In addition to topology changes, the characteristics of the selected components have an utmost importance regarding the efficiency. While defining the FETs, Inductor and Filter Capacitor attention must be paid on the parasitic resistance.
    - The FETs' series resistance in "ON" state is called $R_{DS_{"ON"}}$
    - The series resistance of the Inductor and Filter Capacitor is called ESR, (Equivalent Series Resistance)
    - Low forward drop Schottkys

5.2. Synchronous Buck Converter – Basic Schematics

Figure 9 shows the basic Schematics of the Synchronous Buck Converter.

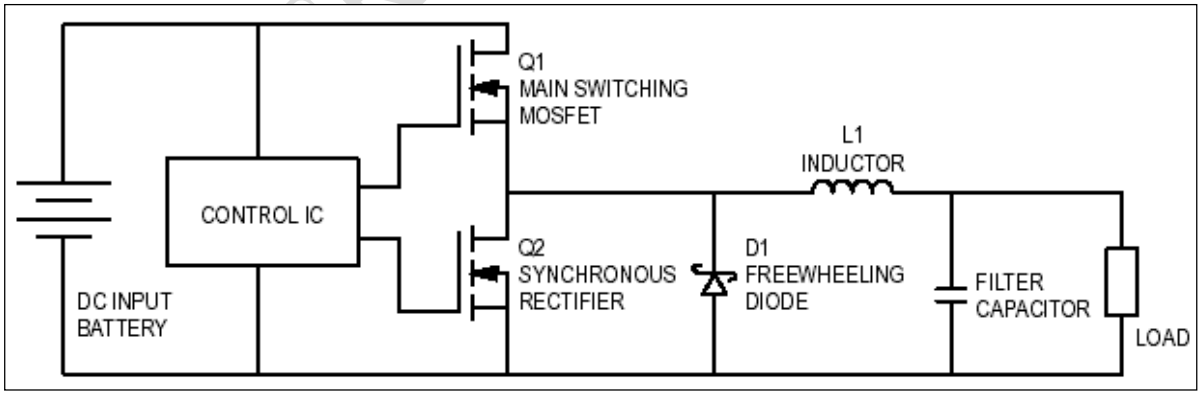

Figure 9: Synchronous Buck Converter with Parallel Schottky Diode

When FET, (MOSFET), Q1 is switched off before Q2 turns on, the free-wheeling diode D1 will provide a continuous path for either the current and the energy stored in inductor L1 to continue flowing through the diode. This waveform is shown below in Figure 10.

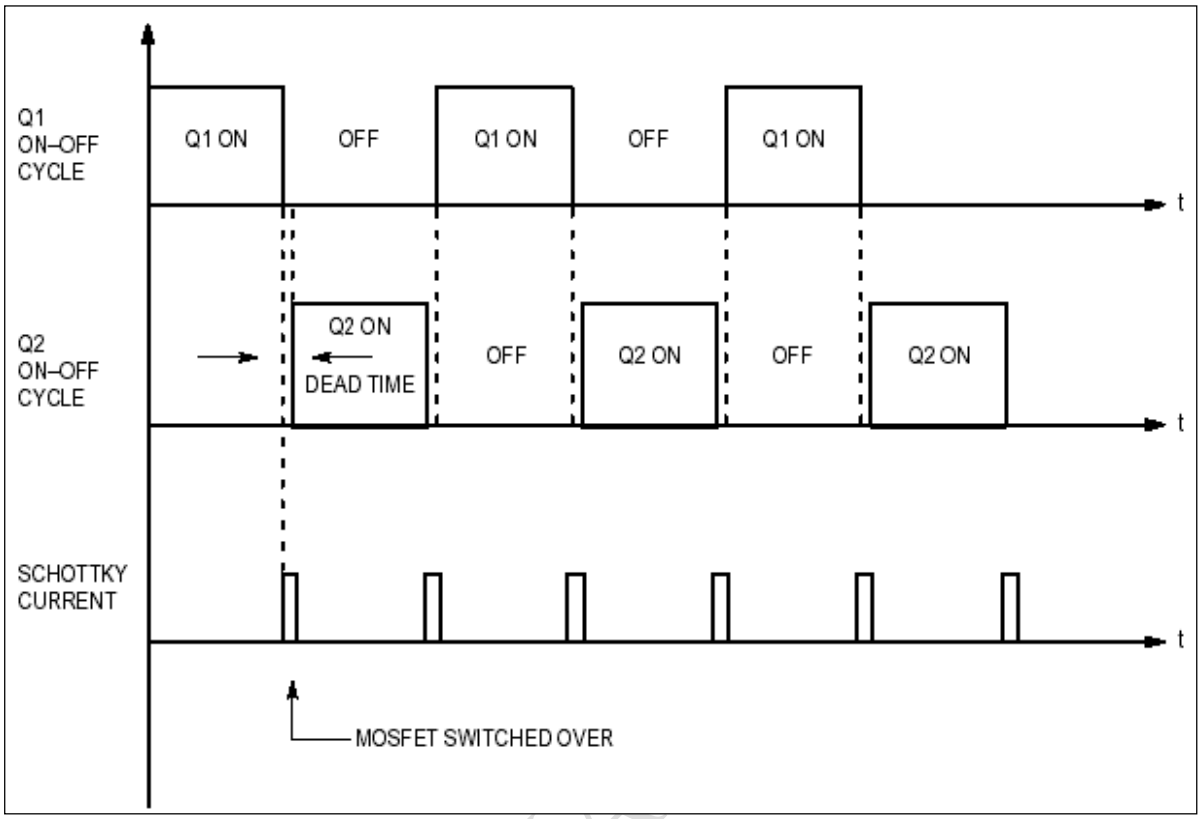

Figure 10: Dead Time and Schottky Diode Waveforms

With the parallel Schottky diode D1 in place, the overall efficiency of the power supply is slightly improved. The comparison of efficiency between Synchronous Rectifier with a Parallel Schottky Diode and that of a Schottky Diode alone is shown in Figure 11.

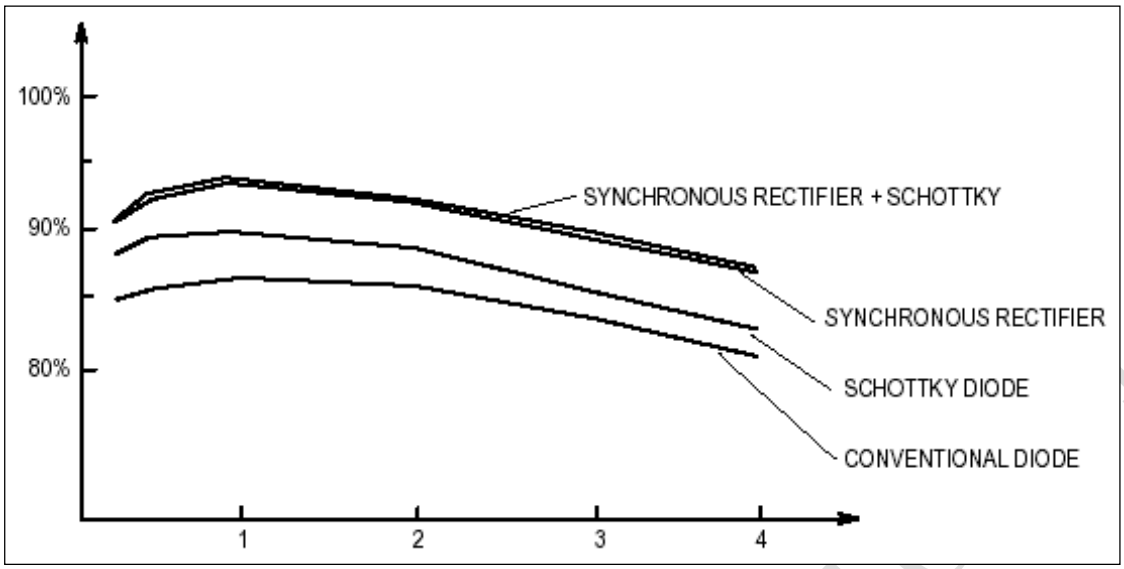

Figure 11: Efficiency Improvement by employing Synchronous Rectification

5.2.1. Further Improvements

In order to improve the efficiency losses in the converter should be reduced by applying the following:

- Increase the turn-on and turn-off switching speed of the MOSFETs' triggering gate pulses to reduce the switching loss during transition
- Reduce the switching frequency of the converter, which lead to the reduction of the transitions during a single time unit.
- As stated earlier, use low internal resistance components

The switching loss of the MOSFET is shown in Figure 12.

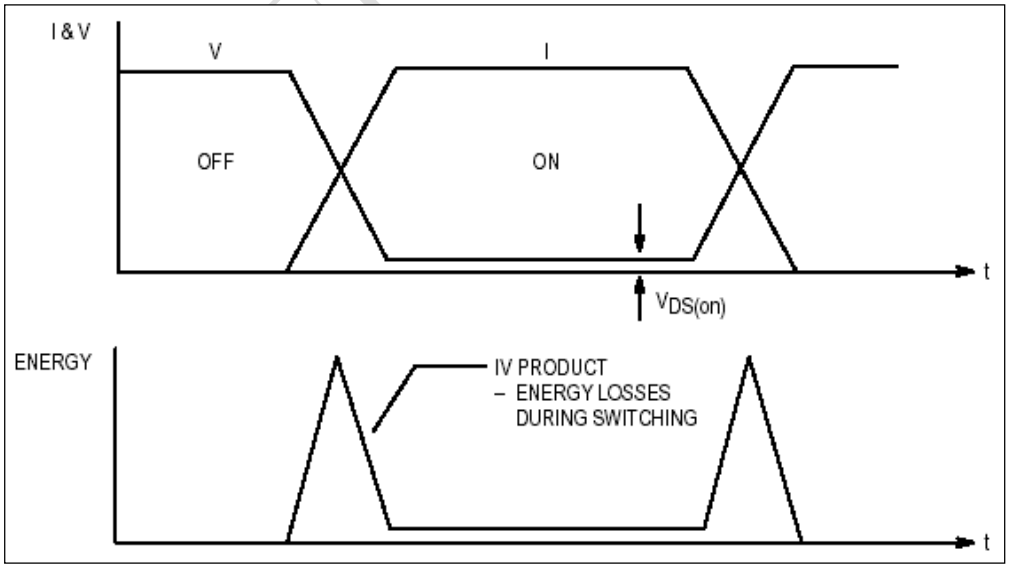

Figure 12: Switching Loss of MOSFET during transition

5.2.2. PWM Output Voltage Control Loop

In order to control the output voltage which is influenced by the input voltage variations and load variations, a Voltage Controlling Loop is used as part of the PWM controller circuitry.

Figure 13 shows how this is done:

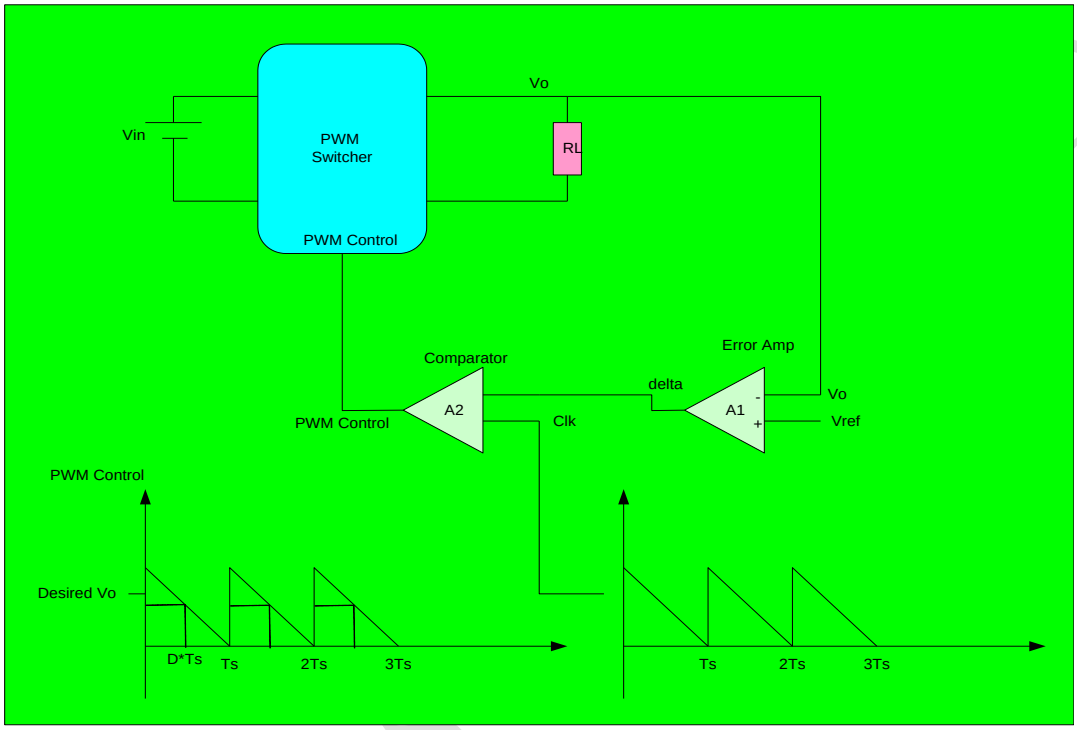

Figure 13: PWM Output Voltage Control Loop

The Error Amplifier's operation resembles the error amplifier of the LDO shown in Figure 1.

The output of A1 is varied depending on the voltage difference between the (+) and the (-) terminals. A2, is a comparator that outputs "1" and "0" depending on the time durations in which the "delta" level compared to the "Clk" level. The pulse width will widen as long as the output voltage is low and vice versa.

5.2.3. Available PWM Controllers in the DC/DC converter Market

Many manufacturers such as TI, National, Linear, Onsemi, Maxim produce various PWM controllers for various applications. The available Synchronous Buck Converter can be divided into two groups.

5.2.3.1. PWM Controllers with External FETs

Figure 9 shows that in order to design a Synchronous Buck PWM DC/DC Converter, there is a need in two FETs. These controllers require the addition of these FETs externally, which of course increase the PCB Real Estate demands for the application.

The advantage in this case is the ability to work with higher currents, assuming the proper FETs are chosen.

In addition, multiple output PWM Controllers with external FETs are available.

5.2.3.2. PWM Controllers with Internal FETs

As one can assume, these controllers have embedded FETs, hence it saves valuable PCB Real Estate. The disadvantage of this controller is that it is aimed only for a restricted amount of current and power. In addition, the series resistance of the internal FETs is relatively high.

6. Synchronous Buck Converter design from SCRATCH

6.1. Forward

This chapter is very technical and straightforward. All steps in Synchronous Buck DC/DC Converter design are summarized from the first calculation to the last.

Naturally, common sense should be used on finalizing the design.

6.2. Designing a Synchronous Buck Converter

6.2.1. Choosing the Switching Frequency

The following parameters have an effect on the switching frequency definition:

6.2.1.1. PCB Real Estate:

As mentioned in Clause 2.2.3, as the frequency rises, the inductor size decreases.

6.2.1.2. Efficiency:

The higher the frequency, the greater are the switching losses. Clause 5.2.1

6.2.1.3. Controller Switching Frequency Range

Depends on the chosen PWM Controller.

6.2.1.4. Duty Cycle, (Vin vs. Vout)

The switching frequency is based on the minimum duty cycle ratio

$$\frac{V_{out\min}}{V_{in\max}} = \frac{t_{"ON"}}{T} = f \cdot t_{"ON"} = D_{\min}$$

Equation: 7

6.2.1.5. Current Limit Propagation Delay to Output

In order to maintain current limit capability, the minimum "ON" time of the upper MOSFET, must be greater than $t_{"ON"}$, hence using Equation 7 and the latter inputs will lead to Equation 8.

$$f_{\max} = \frac{(\frac{V_{out\min}}{V_{in\max}})}{t_{"ON"}}$$

Equation: 8

A typical $t_{"ON"}$ is 300[ns].

6.2.2. Define Ripple Current – ΔI

Figure 8 shows the changes in the current flowing through the Inductor. A high ripple current will lead to higher EMI but smaller size Inductor and vice versa.

A typical ΔI will be 30% of the nominal current required by the load. For more conservative designs ΔI will be about 10% times the nominal current.

ΔI is the peak-to-peak inductor current.

While selecting the output capacitor, in addition to the parameters defined in Clause 6.2.5, the minimum ripple current of the output capacitor must be equal to or greater than ΔI.

6.2.3. Calculating the Minimum Inductance Value

$$L_{\min} = \frac{V_{out} \cdot (V_{in} - V_{out})}{V_{in} \cdot \Delta I \cdot f}$$

Equation: 9

A typical 25% margin is acceptable, hence the inductance L to be selected will be:

$$L = 1.25 \cdot L_{\min}$$

Equation: 10

6.2.4. Output Voltage Ripple

The Output Voltage ripple is affected by the output capacitance. A typical output ripple ΔVout is about 20[mV] to 50[mV]. Conservative designs require about 10[mV] output ripple.

6.2.5. Output Capacitor Selection

6.2.5.1. Calculating the Minimum Output Capacitance

$$C_{out} = \frac{V_{out} \cdot (1 - D)}{8 \cdot L \cdot f^2 \cdot \Delta V}$$

Equation: 11

6.2.5.2. Calculating ESR of the Output Capacitance

The output capacitor ESR will be calculated by equation 11, and usually in between 30[mOhm] to a few hundreds of mili ohms, depending on the design constraints.

$$ESR_{Cout} = \frac{\Delta V}{\Delta I}$$

Equation: 12

6.2.5.3. Minimum Ripple Current of the Output Capacitor

Note that the ripple current defined on Clause 6.2.2 flow through the output capacitor; hence the capacitor's minimum ripple current must be equal or greater than ΔI.

6.2.5.4. Capacitor Voltage Rating

It's very important to choose an output capacitor with appropriate voltage rating. The voltage rating should be at least 20% higher than the operation voltage – Vout.

7. Layout Guidelines

7.1. Forward

Power generating portions of the layout should be considered first. Second, sensitive nodes in the layout that are susceptible to interference.

An efficient power-supply layout limits EMI and RFI by having small ***high-current loops***, proper grounding of the control stage, and strategically sized traces to handle peak currents

7.2. Small Current Loops

Controlling current flow is of the utmost importance. Small current loops achieve two things:

1. They generate less radiation
2. They produce less magnetic coupling between adjacent circuitry

Figure 14 shows the main source of EMI in a Buck Converter power supply.

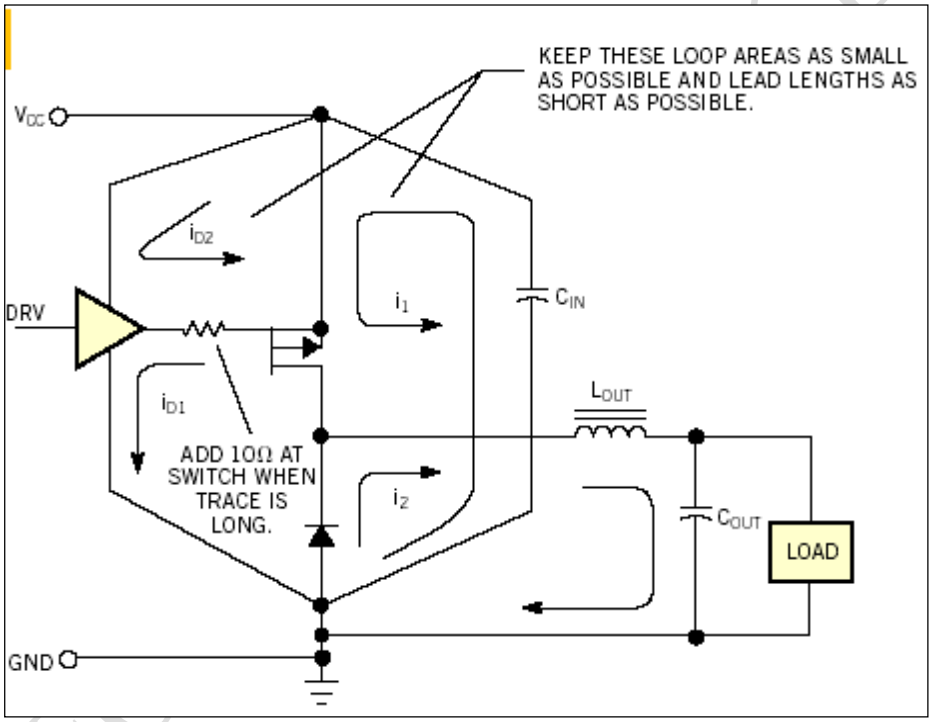

Figure 14: Main source of EMI in a Buck Converter

In other words, the placement of the input capacitor should be close as possible to the upper FET and the controller. The lower FET, inductor free-wheeling diode and the output capacitor should be as close as possible to each other and the controller as well.

7.3. Control Stage – Noise Sensitive

The feedback signal of the power supply's controller is very sensitive to noise pickup.

One end of the trace connects to a low impedance node, which is the output rail or a resistive divider at the output. The other end connects to the feedback pin, which is the high impedance input of the error amplifier. If this trace picks up noise, (capacitively or inductively), as it passes between these two nodes, it can lead to erroneous output voltages, and in extreme cases even instability or device failure. Figure 15 relates to the feedback issue.

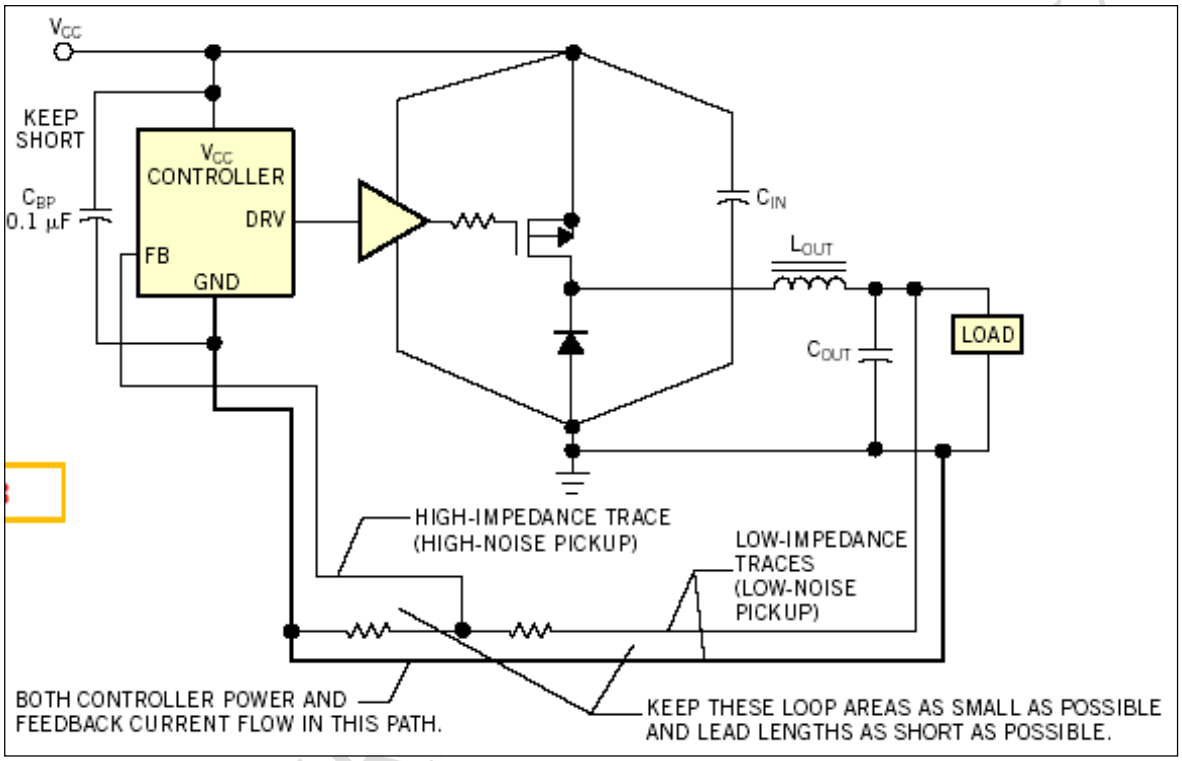

Figure 15: Feedback Signal Routing

There seem to be two options for this:

1. Keep the feedback trace short if possible so as to minimize noise pickup AND/OR
2. Keep it away from noise sources (e.g. switching diode, inductor)

Keeping the trace short may not be feasible. In fact **the feedback trace may be deliberately kept slightly longer so as to route it away from potential noise sources. It should not pass under the inductor or diode in particular**.

If a double-sided SMT board is being used, a good strategy is as follows:

- Use a via at the output resistive divider to bring the trace to the other side.
- Run the trace to cut through the surrounding ground plane areas, taking care not to pass it under the inductor/diode and not parallel to any power trace on either side of the board (though it can cross them perpendicularly)
- And then very close to the IC, use another via to bring out the trace to the component side where it connects to the feedback pin of the IC.

Refer to Figure 16, (a), which shows the situation for the Adjustable part. The trace, which picks up noise, is bold. However, if we consider fixed voltage part, we learn an important thing. This is in Figure 16 (b). Note that the feedback trace here is not marked in bold. The reason is that **a trace can pick up noise only if at least one end of it is a high impedance node**. In Figure 16 (b), the feedback pin goes to a resistive divider rather than directly to the input of the error amplifier. So, it is relatively immune to noise pick up. The only section where noise can be picked up is inside the IC, shown in bold, and this is a very short path. Applying the same principle to an adjustable part provides another interesting way to route the feedback trace. One way is shown in Figure 16 (c). Here the length of the "feedback trace" is very short, so it is relatively noise-free. The feedback resistors are physically close to the IC and the trace from the output to the upper resistor has low impedances on either side, and does not pick up noise. However, the connection of the lower resistor to ground is not ideal as the resistive drop across the section marked "Io*R" will affect the output voltage load regulation slightly.

Another way is in Figure 16 (d), and this solves both issues. This is therefore recommended. If a ground plane is used however, both figure 16 (c) and 16 (d) are actually the same if vias are correctly placed to couple into this plane. For Figure 16 (d), if possible, it is a good idea to run the top and bottom traces to the resistive divider parallel and close to each other, so as o minimize any further chance of noise pickup.

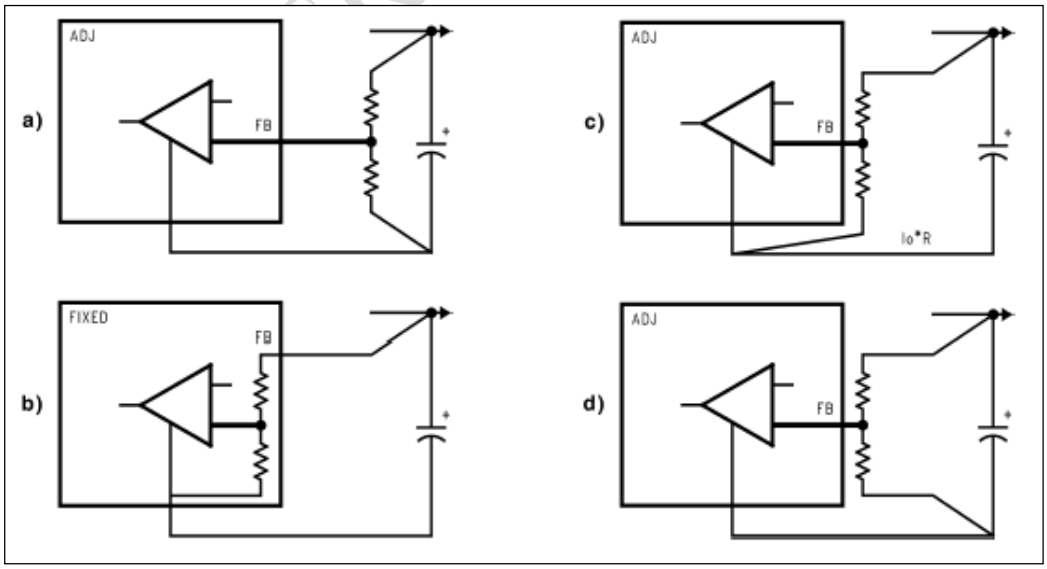

Figure 16: Feedback Traces (bold lines susceptible to noise

7.4. Ground Control

Much effort should go into not breaking or partitioning this plane. Further, in general, if too much swinging power flow occurs through such a plane, it can create “ground bounce” and cause controller upsets. Therefore in higher power applications, with the added luxury of multi-layer PCBs, separate **Signal Ground** and **Power Ground** planes are used.

In addition there should be a **Digital GND**. The Power Ground should be connected to the Digital Ground at one point of connection through vias or a wide trace, which operates as an inductor that filters the switching noise harmonics. The Signal Ground should be connected to the Power Ground at a single point of connection.

7.5. Output Voltage Planes

The output of the PWM Switcher is usually fed into the components on the PCB via the VCC planes. The common tendency is to increase the VCC plane as much as possible in order to reduce the plane impedance and to strengthen the VCC and GND planes capacitive coupling.

But, keeping in mind the high power switching areas where the PWM Switcher is employed on the PCB, the designer’s motivation should be to narrowing down the output VCC plane to the minimum under this area. The VCC plane should start only at the output capacitor Co stage and then spread along the PCB.

It’s important to remember that increasing the VCC plane area might end with negative consequences in this case.

7.6. Layout Example

Figure 17 shows the schematics of the TPS40055 Evaluation Board by TI, (document SLUU190)

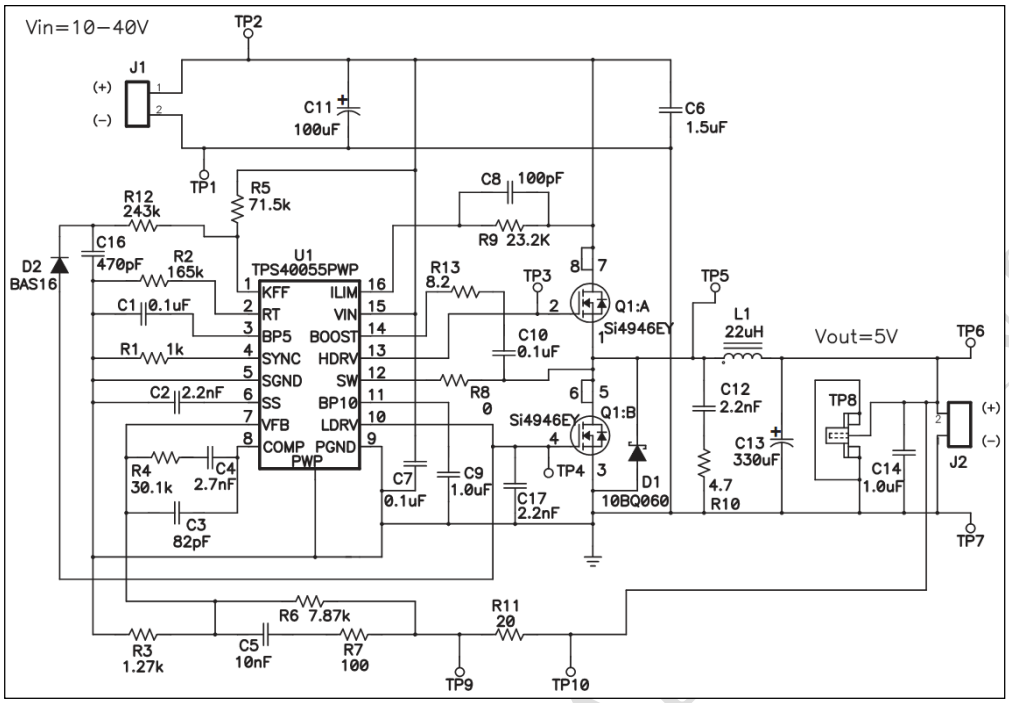

Figure 17: TPS40055 Evaluation Board Schematics by TI

Figure 18 Shows the Top Side Component Assembly of the Evaluation Board.

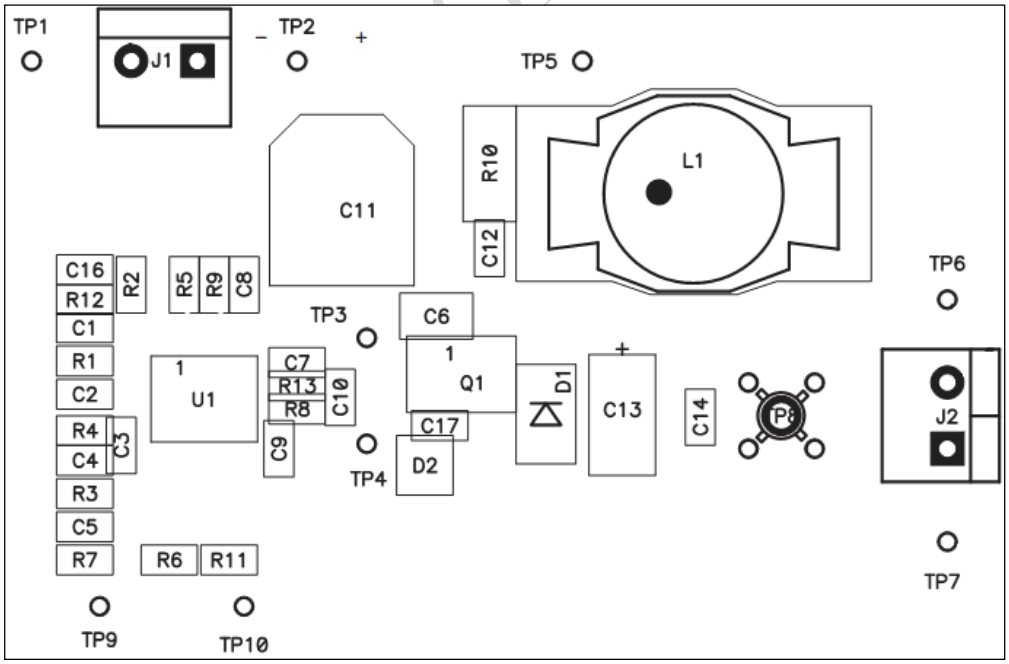

Figure 18: Top Side Component Assembly

Figure 19 shows the application of the layout guidelines discussed previously. The Signal GND is connected to the GND, (Power GND – since this is an Evaluation Board and there is no other Digital GND), in a single point, which is pin 9.

The "Intentional Cut" is made in order to separate the high switching area on the Cout capacitor from the output connector.

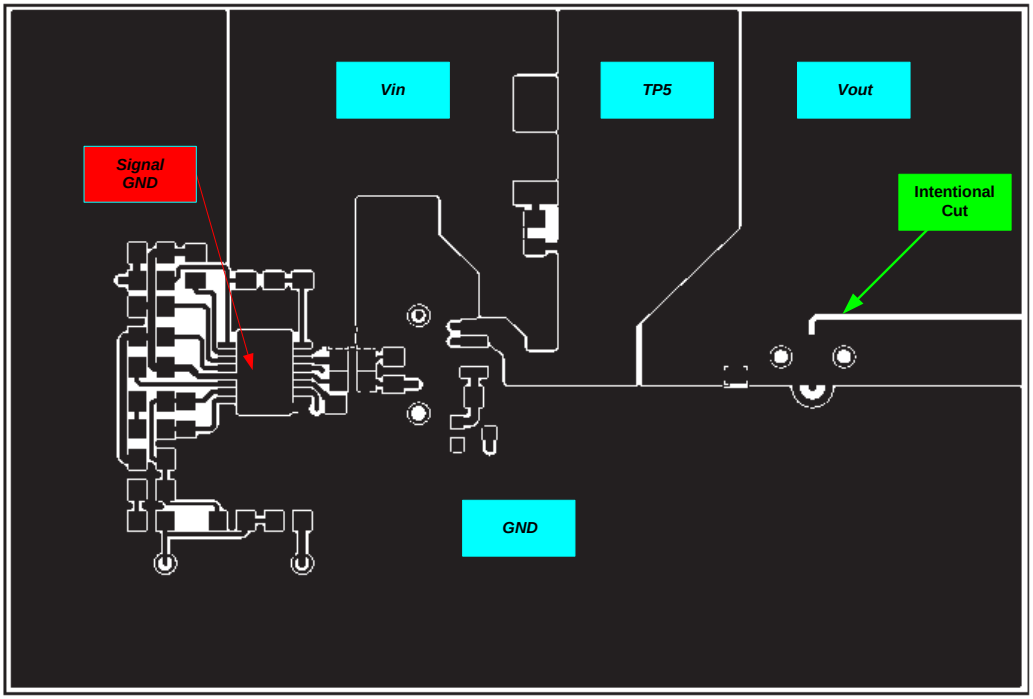

Figure 19: Top Layer Copper

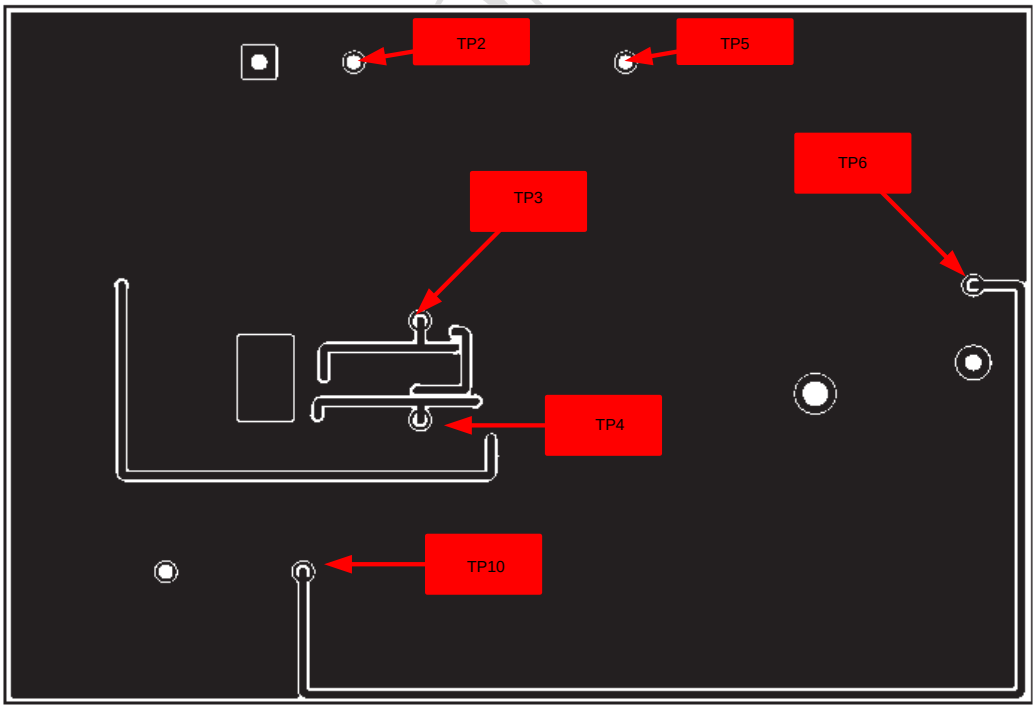

Figure 20: Bottom Layer Copper